Temperature-Dependent Testing of Electro-Optic Integrated Circuit (E-PIC) Wafers

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May-2025
AN5525-1.0

EXECUTIVE SUMMARY

The rapid evolution and adoption of Electro-Optic Integrated Circuits (E-PICs) have redefined performance benchmarks across a wide spectrum of next-generation technologies. From high-speed optical communication and artificial intelligence to quantum computing and advanced IoT architectures, E-PICs are at the core of innovation. Their application scope continues to expand, now extending into mission-critical and harsh-environment sectors such as autonomous transportation, aerospace, and medical diagnostics, where precision, durability, and miniaturization are paramount.

In response to this growing complexity and diversity of use cases, wafer-level characterization has emerged as a mission-critical process in the E-PIC development lifecycle. Comprehensive testing at the wafer level enables early detection of performance deviations, ensures long-term reliability, and supports compliance with increasingly rigorous industry and regulatory standards. As manufacturers scale production and integrate E-PICs into high-value systems, accurate, high-throughput wafer-level metrology becomes indispensable—not only to reduce time-to-market but to maintain competitive advantage in a rapidly evolving ecosystem.

This application note highlights the importance of temperature testing E-PIC devices at every stage of the manufacturing process—from wafer to packaging. It offers practical guidance on setup optimization, hardware selection, and measurement techniques to minimize signal loss and maximize measurement accuracy. Real-world test scenarios illustrate best practices for reducing parasitic effects and enhancing data integrity during on-wafer measurements.

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INTRODUCTION

At first glance, Temperature-Dependent Testing (TDT) of Electro-Optic Integrated Circuit (E-PIC) wafers may seem excessive; however, it is a critical step in ensuring long-term reliability and meeting product qualification requirements.

E-PICs are increasingly deployed in high-performance, long-lifecycle applications such as telecom, datacom, precision sensing, aerospace, and defense. These environments demand robust reliability under thermal stress. TDT accelerates aging by exposing devices to repeated heating and cooling cycles, effectively simulating years of field use within a shortened test timeframe. This helps reveal early indicators of failure before they become costly issues.

Thermal cycling stresses interfaces between materials with different coefficients of thermal expansion. E-PICs often incorporate a complex stack of materials, including III-V semiconductors, silicon, dielectrics, metals, and adhesives. Each material responds differently to temperature changes, potentially resulting in micro-cracks, delamination, or fatigue in waveguides, bond layers, or metallization.

TDT helps detect:
- Stress at material interfaces
- Cracking in bonding or passivation layers
- Misalignment in optical paths caused by micro-shifts

For E-PICs intended for packaging—especially hermetic or fiber-attached configurations—TDT becomes even more important. Components such as fiber-attach adhesives, flip-chip interconnects, CPO I/O Optical Engines and die-attach materials can deform or degrade under thermal stress conditions. Testing early in the development process helps ensure that the complete device stack, not just the die, will perform reliably in the field.
Thermal shifts can subtly impact key optical and electrical parameters over time. TDT can help validate:
- Wavelength and power stability over 1,000+ cycles
- Polarization consistency
- Insertion loss versus wavelength stability
- Functional device performance at deployment temperatures

Meeting qualification standards is often non-negotiable. Industry protocols such as Telcordia GR-468 and MIL-STD-883 require rigorous environmental testing—including TDT—as part of their qualification criteria. Performing TDT during early development minimizes the risk of failure during final system-level testing.

Even in R&D, TDT provides valuable early feedback. Whether validating new structures or materials, temperature cycling can identify temperature-related performance and reliability issues before production ramp-up. Testing early can save time, reduce risk, and support a smoother path to market.

This application note explores how MPI's automated probe stations can address these challenges. It provides practical guidance on system configuration, component selection, and measurement optimization. Applying these techniques can help minimize measurement uncertainty, improve data reliability, and accelerate time-to-market for high-performance E-PIC devices.

PROBLEM STATEMENT / TECHNICAL CHALLENGES

1. **Temperature-induced performance drift** is a critical reliability concern in Electro-Optic Integrated Circuits (E-PICs). Depending on the device type and architecture, thermal variations can lead to:
   - **Insertion Loss (IL) fluctuations**
   - **Laser instability or mode hopping**
   - **Polarization-Dependent Loss (PDL) shifts**
   - **Return Loss (RL) degradation**
   - **Detector instability or noise increase**

   Regardless of the E-PIC's application, these effects can significantly degrade system-level performance and lead to functional failures in the field.

2. Ambient-only testing is insufficient. Although an E-PIC may pass parasitic and functional tests at room temperature, its behavior can change significantly under real-world thermal conditions. This can result from:
   - System-induced temperature changes (e.g., self-heating, adjacent electronics)
   - Environmental exposure (e.g., outdoor, aerospace, automotive applications)
   - As a result, testing across a broader temperature range beyond expected use conditions is essential for performance validation and qualification.

3. **Material-level thermal mismatch** is a key contributor. In particular:
   - Thermal expansion and contraction of glass, silica, and other optical-interconnect materials can change the physical displacement between interconnects.
   - These effects are especially pronounced in complex multilayer 2D/3D E-PIC architectures and in E-PICs built on glass or silica interposers, where multiple material interfaces can amplify thermal stress.
   - The resulting micro-shifts and interface stress can alter optical-path alignment, reduce coupling efficiency, and degrade waveguide integrity.

4. **Calibration discrepancies arising from thermal differences between the calibration setup and the wafer under test.**
   - Optical calibration is typically performed at ambient temperature, whereas the wafer under test may be evaluated across a much wider temperature range. Differences in temperature and material coefficients can introduce measurement inaccuracies due to expansion and contraction of the wafer under test.

THERMAL EXPANSION SOLUTION OVERVIEW

Solutions can be divided into three groups:

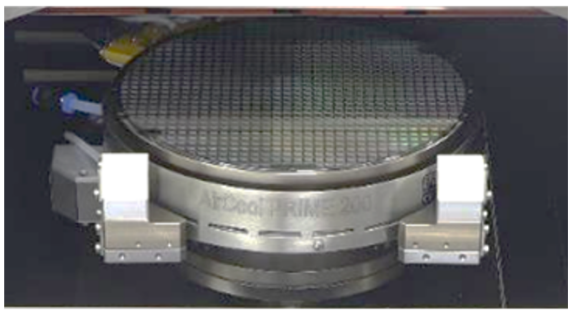
1. **On-Wafer Chuck with Integrated Temperature Testing**
   Due to its integrated design, this setup is recommended for most applications requiring optical testing in the range of −50°C to +200°C. Key advantages include:
   - **Simplified operation** – The integrated design minimizes system complexity and eliminates the need for external plumbing, hydrogen tanks, or other auxiliary equipment.
   - **Automation** – The integrated temperature-controlled setup enables operator-free testing without requiring the wafer under test to be moved to another location or system.
   - **Regulatory compliance** – The system minimizes or eliminates the need for special permits associated with external cooling or heating solutions, simplifying compliance with applicable local environmental and safety regulations.
   - **Efficient thermal testing** – The integrated design minimizes thermal mass, enabling faster temperature ramp-up and cool-down times, lower energy consumption, and improved test throughput.
   - **Self-contained air circulation** – Temperature-controlled air is continuously circulated within the system, minimizing the risk of ice and water buildup during low-temperature testing.
   - **Lower CAPEX and OPEX** – Capital and operating costs are significantly lower compared with external temperature-control solutions.
   - **Reduced footprint** – The integrated design eliminates the need for external temperature-control equipment, resulting in a more compact and efficient overall test setup.
   - **Improved test consistency** – Integrated temperature control provides a controlled and repeatable thermal environment, supporting more consistent measurements across devices, wafers, and test runs.
   - **Field upgradable** – Several chuck models are available and can be replaced in the field depending on the testing requirements and DUT needs.

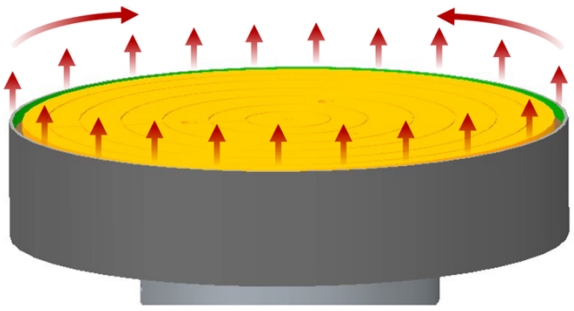
2. **External chamber temperature testing.**
   This approach requires the entire probe system to be temperature-controlled and placed within a dedicated chamber or temperature-controlled room.
   Although this is a commonly used setup, as noted in solution 1, it presents several disadvantages compared to an integrated solution—except for temperature range. If temperature testing needs to extend beyond -50°C to +200°C, this becomes the preferred solution. This setup is particularly relevant for wafer testing in quantum photonic applications, as explained below.

3. **Quantum temperature testing at 4 K levels, which can be implemented using three approaches:**
   - **Dedicated cryogenic probe system.**
     The main disadvantages of a dedicated cryogenic wafer probe system are CAPEX and OPEX, both of which are significantly higher than the alternatives. MPI currently does not offer this solution because lower-cost alternatives can address the use case, as described below.
   - **Standard E-PIC probe system positioned in external chamber.**
     This approach requires the entire probe system to be temperature-controlled and placed within a dedicated chamber. A temperature-controlled room, as described above, cannot be used.
     As with dedicated cryogenic probe systems, both the CAPEX for the chamber and setup, as well as the OPEX, are significant. Cooling a wafer from ambient to sub-Kelvin levels is both time- and energy-intensive, often requiring up to 24 hours to reach the 4–77 K range from ambient temperature.
     Maintaining calibration accuracy across this extreme temperature range presents additional challenges, which will be addressed in a dedicated application note.
   - **On-wafer chuck with integrated temperature testing**
     Using a standard E-PIC probe system with a small external cryogenic temperature chamber. In this approach, the quantum photonic wafer is first tested between −50°C and +200°C using a standard probe system, as described in solution 1. Once sliced, a single die from the same wafer is then randomly selected and tested in a small external cryogenic chamber at 4–77 K.
     The die's performance at cryogenic temperatures is then cross-correlated with its behavior at higher temperatures to establish pass/fail criteria.
     For example, if a wafer contains 100 E-PICs that all meet specifications at -50°C to +200°C, and one of those E-PICs (as a die) also meets specifications at 4–77 K, the remaining 99 with the same performance measured at -50°C to +200°C, can be considered as passing based on that correlation.

EXPERIMENTAL SETUP

- **On-wafer chuck with integrated temperature testing.**
  The core of the system is the MPI & ERS PRIME™ Thermal Chuck with patented AirCool® Technology.

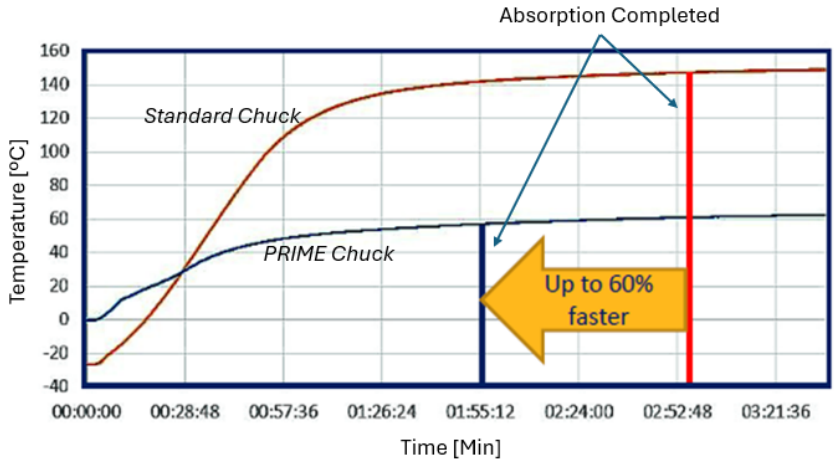




The AirCool® PRIME™ thermal chuck features a NanoChamber, which sits atop a standard PRIME™ chuck base, as illustrated above. The NanoChamber includes a heater that is shielded from the top plate by an isolation layer. Clean Dry Air (CDA)—either air or nitrogen—is introduced from the bottom to maintain consistently dry conditions by preventing moisture from entering the isolation layer. The slightly elevated pressure inside the NanoChamber also helps prevent contamination during the loading and unloading of wafers.

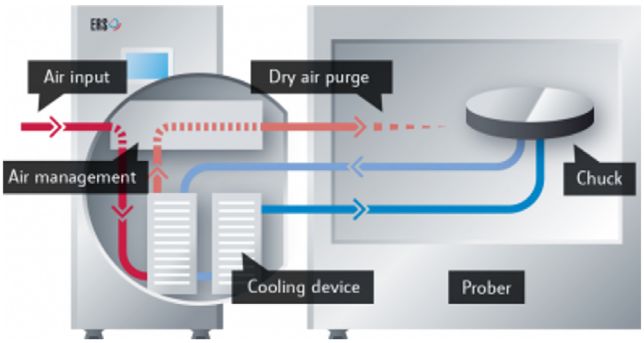
Thanks to the compact size of the NanoChamber, the amount of inert gas (e.g., nitrogen) required to prevent pad oxidation at high temperatures (>200°C) is significantly reduced compared to conventional chamber-based setups.

To minimize OPEX and thermal cycling time, the NanoChamber is designed to reduce the time required for the chuck and wafer to reach the target temperature. Its enclosed environment can reduce temperature absorption completion time by as much as 60%.

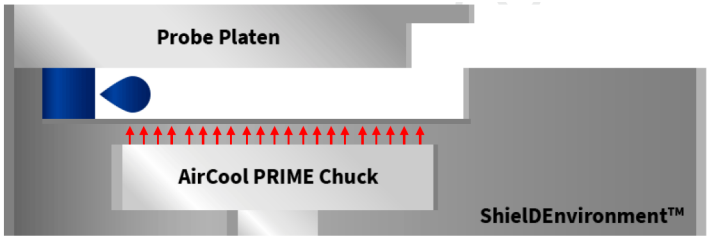


Air management is handled by an ERS chiller, as illustrated below, with automated process-software control.





In addition, temperature control of the top platen—which holds the optical and electrical positioners—is essential for maintaining calibration and ensuring measurement accuracy and repeatability. All MPI semi-automated probe systems feature embedded, software-controlled probe platen air cooling as shown below.

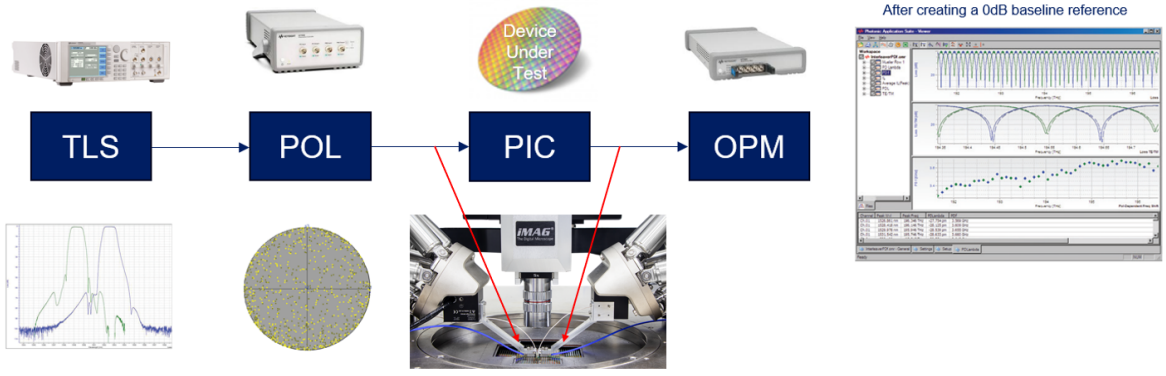


MEASUREMENT PROCEDURE

- After the initial setup and probe alignment using SENTIO®'s automated process, the first step is to complete the temperature calibration process.
  SENTIO® uses an automated, logic-driven process that calibrates the optical fiber probe relative to the wafer under test by establishing the fiber-to-DUT height, angular orientation, and optical power reference. The calibration is performed using dedicated SiPh calibration hardware and can be temperature-dependent, compensating for mechanical expansion and contraction. Once calibrated, SENTIO® applies the stored positional offsets during automated die-to-die testing, ensuring consistent fiber placement and optical measurement conditions across the wafer and over temperature.



- At ambient temperature, an optical insertion-loss-versus-wavelength reference is established using the setup shown below. During this process, the wafer is replaced by a direct connection between the two fiber probes. This can be achieved either by connecting the output fiber from the polarization controller directly to the fiber connected to the optical power meter or by positioning both fibers on a straight waveguide on the wafer.
  Establishing this reference converts absolute optical power values into a relative 0 dB wavelength baseline.



- Once the baseline reference is established, IL and PDL versus wavelength measurements can be performed at various temperature settings. Depending on the device and measurement setup, other parameters can also be evaluated as a function of temperature, including response time, BERT, phase change, S-parameters, and more.
  Variations in measurement results at different temperatures reveal the temperature sensitivity and temperature dependency of the wafer (E-PIC) under test.

CONCLUSION

While there are several methods for temperature-dependent testing of electro-optic wafers, reliable and actionable data ultimately depends on hardware precision, calibration accuracy, and measurement consistency. Simplicity and system integration are key to achieving repeatable results.

REFERENCES

- MPI Pat-19-020, Method for Compensating for Distance Between Probe Tip and Device Under Test After Temperature Changes.

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